Journal of Physical Sciences, Vol. 11, 2007, 185-198

Design and Implementation of a Hard Disk Drive Read/Write Head Controller Using FPGA for Optimal Performance

Thummeti Buchi Reddy* and M. J. Nigam**

*Department of Electronics and Computer Engineering,
Indian Institute of Technology Roorkee, Roorkee, INDIA-247667.
Email : tbuchireddy@yahoo.co.in.

**Department of Electronics and Computer Engineering,
Indian Institute of Technology Roorkee, Roorkee, INDIA-247667.
Email : mkndnfec@iitr.ernet.in.

Received June 25, 2007; accepted August 10, 2007

ABSTRACT

Many automatic control systems utilize digital control algorithms for the control of desired plant. Fast processing in recent microelectronics components and flexibility inherent for all these programmable solutions gave favor to digital control applications from software-hardware solutions using FPGA. This paper investigates an FPGA-based PID control system for Hard Disk Drive read/write system. An attempt has been made to design and implement a feedback control system using FPGA for optimal performance. Ultimately, the optimally controlled movements of Hard Disk Drive read / write head has been achieved.

Key words: *FPGA, Hard Disk Drive read/write system, PID controller, VHDL, Optimal performance.*

1. Introduction

In today's engineering environment, a rapid move from design concept through solution requires suitably defined formal methods, along with effective software support tools. To address this, a reconfigurable technique based on Field-Programmable Gate Arrays (FPGAs) may be applied, which has the potential for greater functionality and higher performance with smaller volume and low power dissipation. The reconfigurable computing has grown to become an important and wide field of research. The operation of each primitive can be programmed, and also the interconnection pattern, computation tasks can be implemented spatially on the device directly from the producing function to the receiving function. Since we can put thousands of reconfigurable units on a single die,

significant data flow may occur without crossing chip boundaries. The main advantages of FPGA are lower development cost, lesser time to market and their ability to be reprogrammed several times.

2. Disk Drive Read/Write System

Hard disk drive provides important data-storage medium for computers and other data-processing systems. The two main functions of the R/W head positioning servo mechanism in disk drives are Track Seeking and Track Following.

Track seeking moves the R/W head from the present track to a specified destination track in minimum time using a bounded control effort. *Track following* maintains the head as close as possible to the destination track center while information is being read from or written to the disk.

2.1 Formulation of the Problem

The problem of Disk Drive Read/Write System[1] is formulated in step by step procedure as:- **Step 1:** The control goals are established (a) to position the reader head accurately at the desired track and (b) to move from one track to another within 50 milliseconds if possible. **Step 2:** Setting the variable to accurately control the position of the reader head (mounted on a slider device). **Step 3:** The disk rotates at a speed between 1800 and 7200 rpm, and the head "flies" above the disk at a distance less than 100 nm. The initial specification for the position accuracy is 1 micro-meter. Thus, we establish an initial system configuration as shown in Fig. 1. This system uses a motor to actuate the arm to the desired location on the disk.

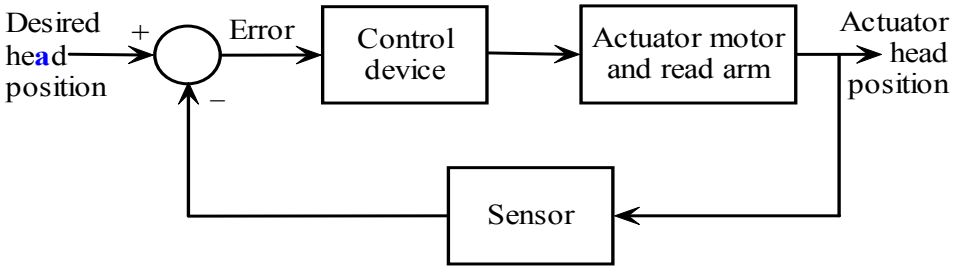

Fig. 1: Closed-loop control system for disk drive.

Step 4: The preliminary system configuration is established. The disk drive reader uses a Permanent Magnet Dc Motor[1] to rotate the reader arm. The DC motor is called a Voice Coil Motor in the disk drive industry. The read head is mounted on a slider device which is connected to the arm. A flexure (spring metal) is used to enable the head to float above

the disk at a gap less than 100 nm. The thin film head reads the magnetic flux and provides a signal to an amplifier. The error signal of Fig. 1 is provided by reading the error from a prerecorded index track. Assuming an accurate read head, the sensor has a transfer function H(s) = 1, as shown in Fig. 2. The model of the Permanent Magnet DC Motor and a linear amplifier is shown in Fig. 2.

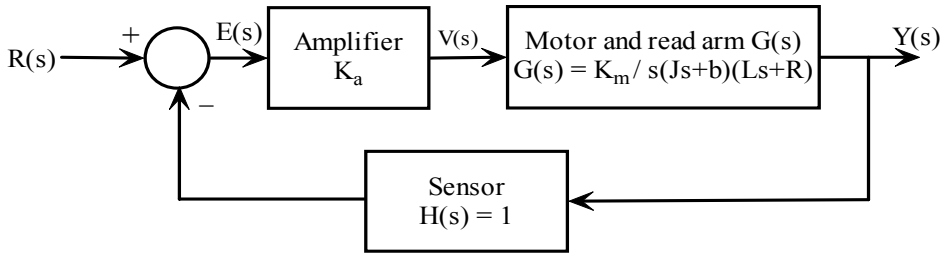

Fig. 2: Block diagram model of disk drive read system.

Table: 1 Typical parameters for disk drive reader[1]

Parameter	Symbol	Typical Value
Inertia of arm and read head	J	1 N.m.s^2/rad
Friction	b	20 kg/m/s
Amplifier	K_a	10 - 1000
Armature resistance	R	1 Ω
Motor constant	K_m	5 N.m/A
Armature inductance	L	1 mH

Typical parameters for the disk drive system are given in table 1. Thus, we have

$$G(s) = \frac{K_m}{s(Js+b)(Ls+R)} \tag{1}$$

$$G(s) = \frac{5000}{s(s+20)(s+1000)} \tag{2}$$

$$\frac{Y(s)}{R(s)} = \frac{K_a G(s)}{1+K_a G(s)} \tag{3}$$

We can also write G(s) as

$$G(s) = \frac{K_m / bR}{s(\tau_L s + 1)(\tau s + 1)} \tag{4}$$

where τ_L= J/b =50 ms and τ = L/R =1 ms. Since $\tau << \tau_L$, we often neglect τ .

Then, we would have

$$G(s) \approx \frac{K_m / bR}{s(\tau_L s + 1)} = \frac{0.25}{s(0.05s + 1)}$$

$$\text{Or} \quad G(s) = \frac{5}{s(s + 20)} \tag{5}$$

The block diagram of the closed loop system is shown in Fig. 3. Using the block diagram transformation we have

$$\frac{Y(s)}{R(s)} = \frac{K_a G(s)}{1 + K_a G(s)} \tag{6}$$

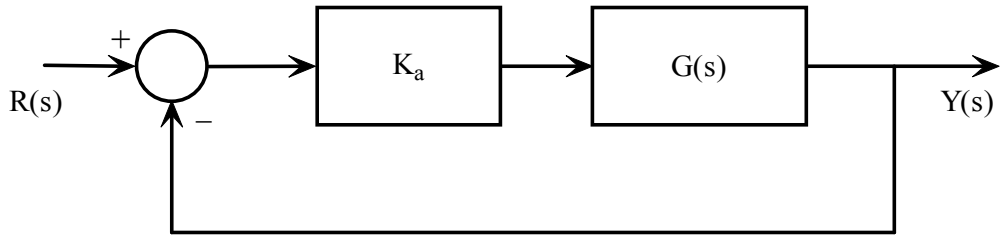

Fig. 3: Block diagram of closed – loop system

Using the approximate second-order model for G(s) we obtain

$$\frac{Y(s)}{R(s)} = \frac{5K_a}{s^2 + 20s + 5K_a} \tag{7}$$

Let the motor mass is M_1 and the head mount mass is M_2. The flexure spring is represented by the spring constant k as shown in Fig. 4(a). The force u(t) to drive the mass M_1 is generated by the dc motor. The simplified model is shown in Fig. 4(b).

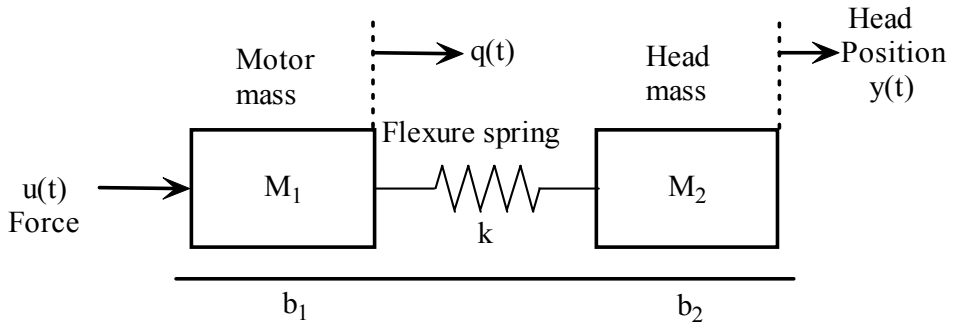

Fig. 4(a): Model of the two-mass system with a spring flexure.

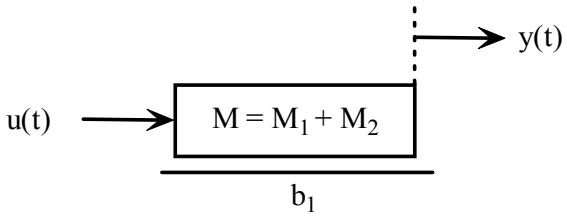

Fig. 4(b): Simplified Model with a rigid spring.

The transfer function model of the head reader, including the effect of the motor coil, is shown in Fig. 5. When M1 = 0.02 kg, M_2 = 0.005 kg, K_m = 125 N-m/A, and b_1 = $410*10^{-3}$ kg/m/s, we obtain

$$G(s) = \frac{Y(s)}{U(s)} = \frac{5000}{s(s+20)(s+1000)} \tag{8}$$

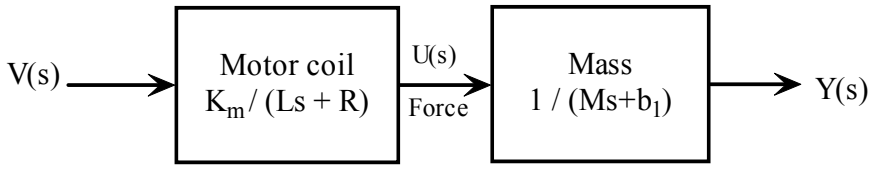

Fig. 5: Transfer function model of head reader device with rigid spring.

Step 5: The design of a disk drive system is an exercise in compromise and optimization. The disk drive must accurately position the head reader while being able to reduce the effects of parameter changes, external shocks and vibrations. The mechanical arm and flexure will resonate at frequencies that may be caused by excitations such as a shock to a notebook computer. Disturbances to the operation of the disk drive include physical block, wear or wobble in the spindle bearings, as well as parameter changes due to component changes. In this section, the performance of the disk drive system is examined to disturbances and changes in system parameters. In addition, the steady-state error and transient response of the system for a step command is examined and the amplifier gain, K_a is tuned. Let us consider the system shown in Fig. 6.

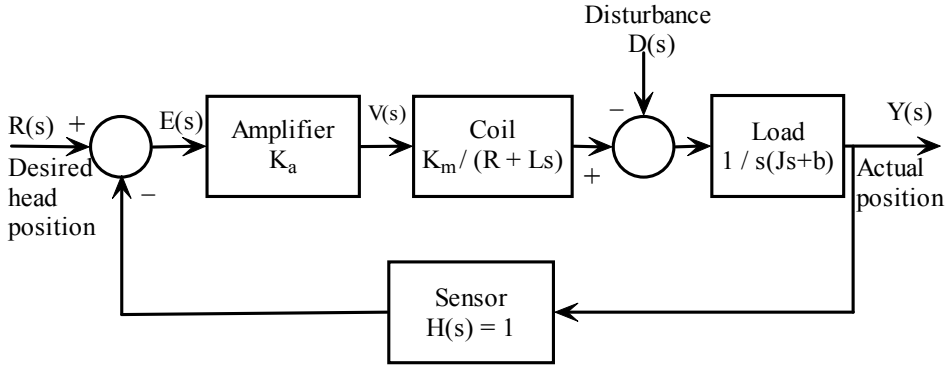

Fig. 6: Control system for disk drive head reader.

This closed loop system uses an amplifier with a variable gain as the controller. Using the parameters specified in Table. 1, the transfer function is obtained as shown in Fig 7.

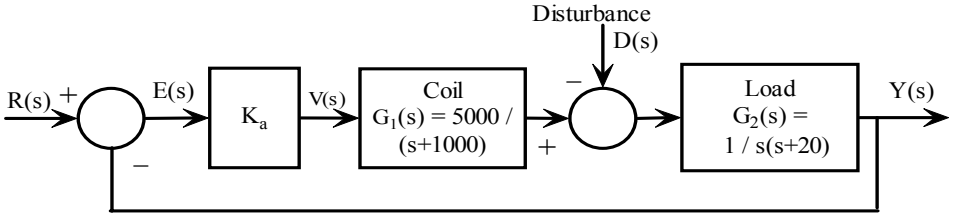

Fig. 7: Disk drive head control system with the typical parameters.

First, the steady state for a unit step input is determined for R(s) = 1/s, when D(s) = 0.

$$E(s) = \frac{1}{1 + K_a G_1(s) G_2(s)} R(s) \tag{9}$$

Therefore,

$$t \xrightarrow{\lim} \infty \;\; e(t) = s \xrightarrow{\lim} 0 \; s\left[\frac{1}{1+K_a G_1(s)G_2(s)} R(s)\right]\frac{1}{s} \tag{10}$$

Then the steady-state error, e(∞) = 0 for a step input. This performance is obtained in spite of changes in the system parameters.

The transient performance of the system is determined as K_a is tuned. The closed-loop transfer function (with D(s) = 0) is

$$T(s) = \frac{Y(s)}{R(s)} = \frac{K_a G_1(s)G_2(s)}{1+K_a G_1(s)G_2(s)} \tag{11}$$

$$= \frac{5000K_a}{s^3 + 1020s^2 + 20000s + 5000K_a} \tag{12}$$

Considering the effect of disturbance D(s) = 1/s when R(s) = 0, (Fig. 7).

$$Y(s) = \frac{G_2(s)}{1+K_a G_1(s)G_2(s)} D(s) \tag{13}$$

2.2 Response with PID controller

Many industrial processes are controlled using Proportional-Integral-Derivative (PID) controllers. The popularity of PID controllers can be attributed partly to their good performance in a wide range of operating conditions and partly to their functional simplicity, which allows engineers to operate them in a simple, straightforward manner. The PID controller is of the following form,

$$G_c(s) = K_p + \frac{K_i}{s} + K_d s \tag{14}$$

The goal is to select K_p, K_i and K_d in order to meet the specifications. The system is shown in Fig.8.

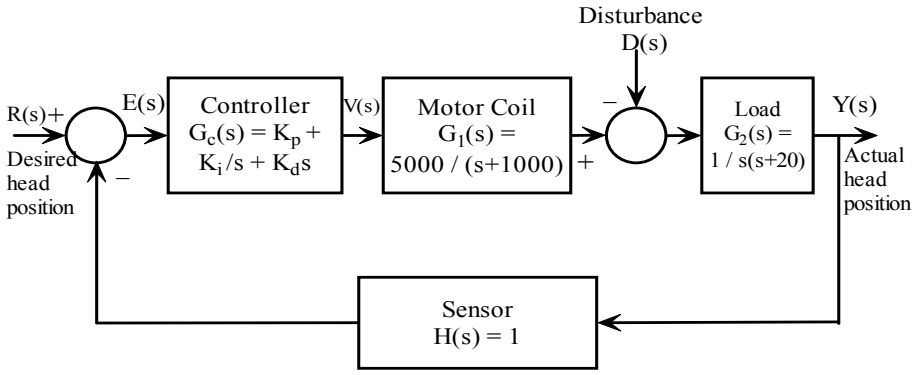

Fig. 8: Disk drive head control system with a PID controller.

The closed-loop transfer function of the system is

$$T(s) = \frac{Y(s)}{R(s)} = \frac{G_c(s)G_1(s)G_2(s)}{1 + G_c(s)G_1(s)G_2(s)H(s)} \tag{15}$$

3. Results and Discussions

The transfer function of the hard disk drive has been formulated and is given by Equation 3. The closed-loop system is shown in Fig. 3. Step responses for different K_a values are shown in Fig. 9. The stability (Nyquist criterion) for different K_a values is shown in Fig. 10.

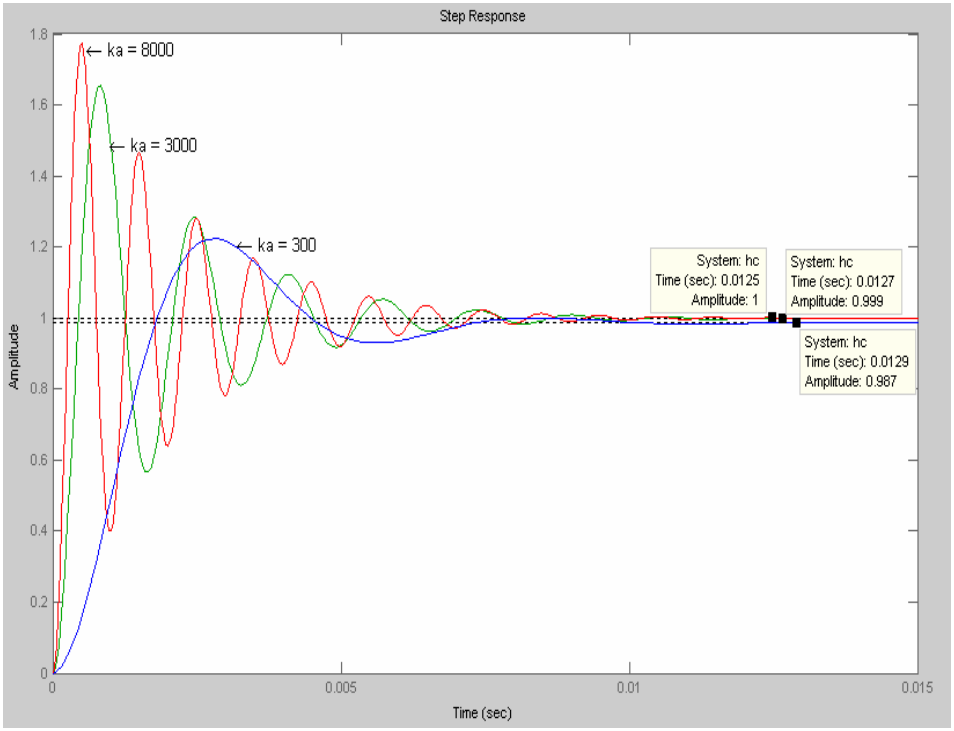

Fig. 9 Step response to equation 3 with different values K_a

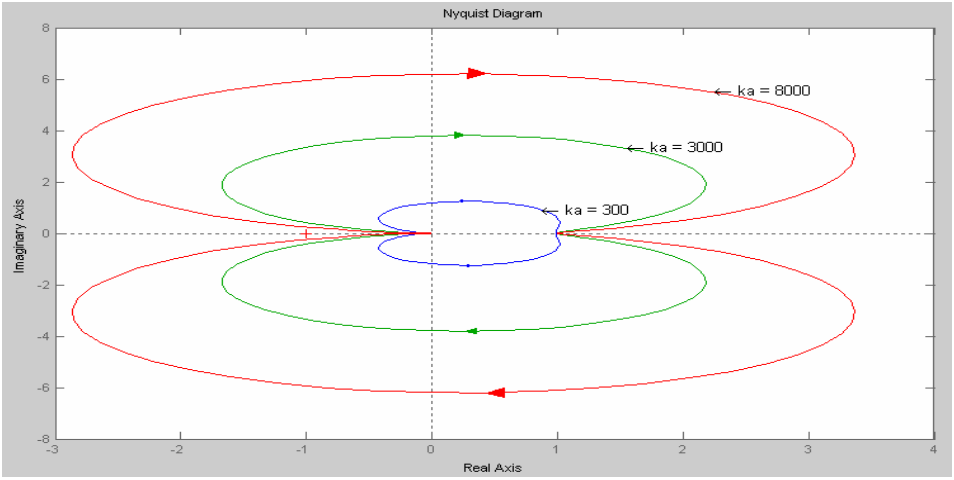

Fig. 10 Nyquist diagram for equation 3 with different values of K_a

3.1 Obtaining the optimal performance

In this section, an attempt is done to tune the amplifier gain K_a in order to obtain the best performance. The goal is to achieve the fastest response to a step input r(t), while (i) limiting the overshoot and oscillatory nature of the response and (ii) reducing the effect of disturbance on the output position of the read head[1].

The desired specifications are as follows:

Desired Values of Performance Measures

• Percent Overshoot less than 5%

• Settling time less than 250 ms

The percent overshoot and corresponding settling time for the different values of K_a are obtained and summarized in Table 2.

Table 2 Response of the equation 3 for a step input

K_a	100	300	1000	3000	7000	8000
Pole Zero location	Left half plane	Left half plane	Left half plane	Left half plane	Left half plane	Left half plane
Percent overshoot(%)	3.8	22	47	66	76	77
Settling time(ms)	8.22	7.17	7.46	7.47	7.55	7.6
Steady state error(%)	3.8	1.3	0.4	0.1	0.1	0

From the results given in Table 2, it is clear that if the desired goals are to be achieved, a compromised gain is to be selected. In this case the gain $K_a = 100$ is selected as the best compromise.

3.2 Response with PID controller

In section 2.2, hard disk drive with PID controller to obtain a desirable response is discussed. Here, MATLAB M-FILE is used to determine the optimal values for PID controller variables. Step response and the stability (Nyquist criterion) of equation 15 for different values of PID coefficients as shown in Fig. 11 and Fig. 12 respectively.

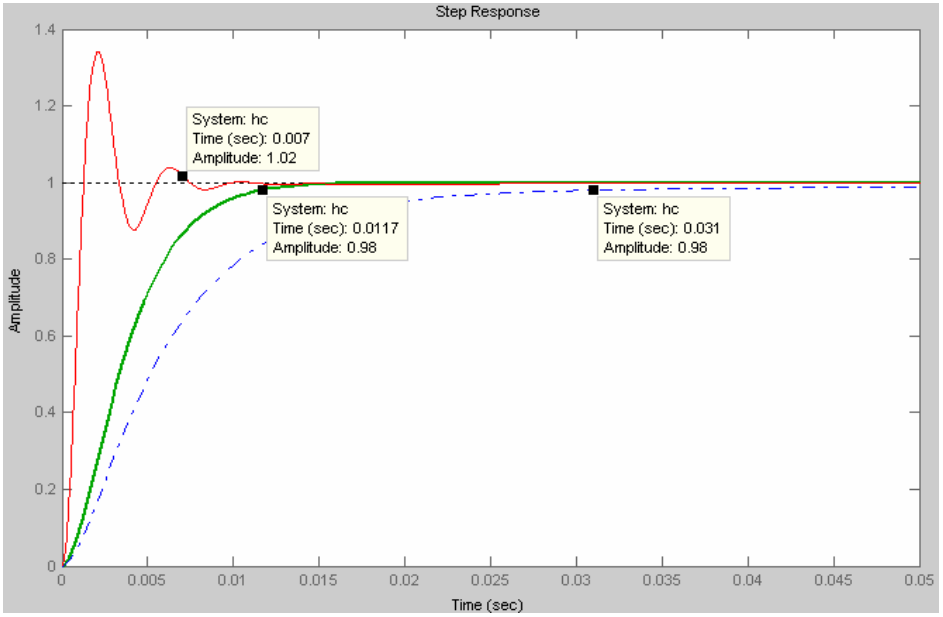

Fig. 11 : Step response to equation 15 by varying the PID coefficients

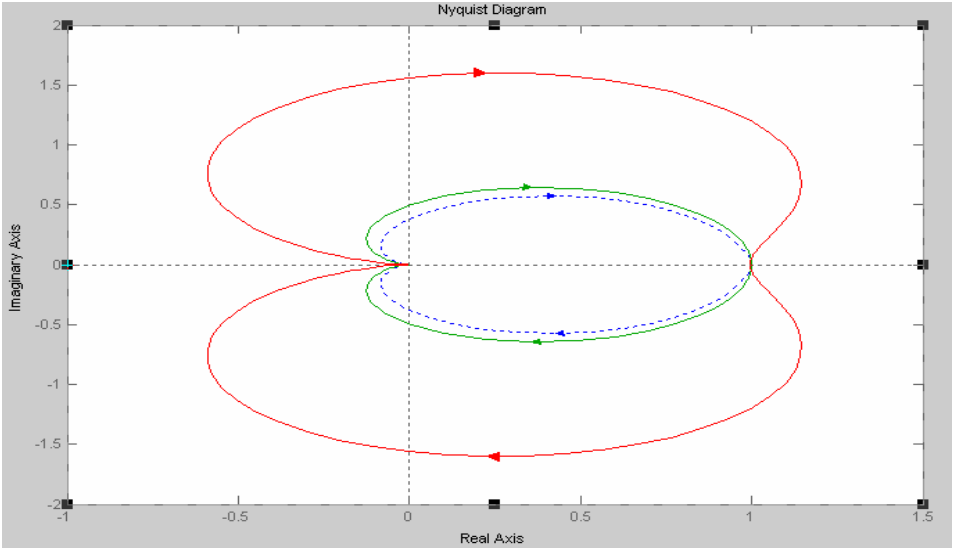

Fig. 12 Nyquist diagram for equation 15 by varying the PID coefficients

3.2.1 Obtaining the optimal performance

The percent overshoot and corresponding settling time for the different values of PID coefficients are obtained and summarized in Table 3.

Table 3 Response of the Equation 15 for a step input

PID Controller	**K_p =500, K_i = 1, K_d = 30.**	**K_p = 1000, K_i = 1, K_d = 50.**	**K_p = 5000, K_i = 1, K_d = 500.**
Pole Zero location	Left half plane	Left half plane	Left half plane
Percent overshoot(%)	0	0	34
Settling time(ms)	31	11.6	6.84
Steady state error(%)	0.1	0	0.3

From the results given in Table 3, K_p = 1000, K_i = 1, K_d = 50 are selected to achieve optimal performance.

3.3 Simulation and Implementation of system on FPGA

The model of the permanent magnet dc motor and a linear amplifier is shown in Fig. 2 and its closed loop transfer function is,

$$\frac{Y(s)}{R(s)} = \frac{5000K_a}{s^3 + 1020s^2 + 20000s + 5000K_a}$$

By converting this equation into discrete domain, the transfer function at $K_a = 100$ is as follows

$$\frac{Y(z)}{R(z)} = \frac{0.01925 * z^2 + 0.02554 * z + 0.0004176}{z^3 - 1.778 * z^2 + 0.823 * z - 3.717e^{-5}} \quad (16)$$

This transfer function (16) is to be simulated and implemented onto the FPGA[2]. The step response is shown in Fig. 13 created by ModelSim.

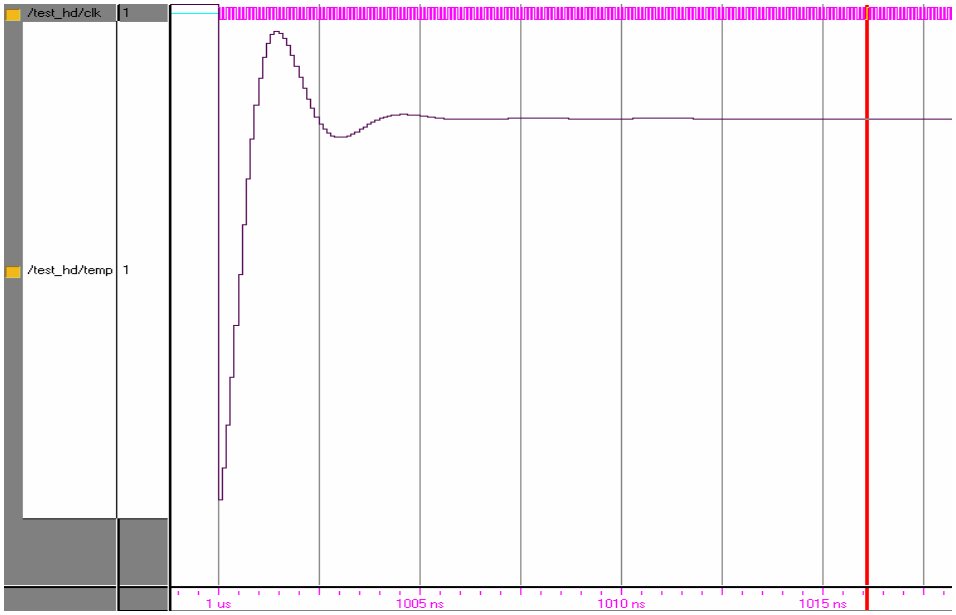

Fig. 13 The step response of equation (16) created by ModelSim

3.3.1 Response with PID controller

In section 2.2, the controller for hard disk drive system is shown in Fig. 8. The corresponding transfer function is given by equation 15, which is reproduced below for quick reference;

$$T(s) = \frac{Y(s)}{R(s)} = \frac{G_c(s)G_1(s)G_2(s)}{1 + G_c(s)G_1(s)G_2(s)H(s)}$$

For, K_p =1000, K_i = 1 and K_d = 50 the above equation becomes

$$\frac{Y(s)}{R(s)} = \frac{250000 * s^2 + 5000000 * s + 5000}{s^4 + 1020 * s^3 + 270000 * s^2 + 5000000 * s + 5000} \quad (17)$$

The characteristics equation is,

$$s^4 + 1020 * s^3 + 270000 * s^2 + 5000000 * s + 5000 = 0. \quad (18)$$

The discrete transfer function of equation (16) is as follows

$$\frac{Y(z)}{R(z)} = \frac{z^3 - 1.301 * z^2 + 0.3012 * z + 8.174e^{-13}}{z^4 - 1.301 * z^3 + 0.3012 * z^2 - 5.636e^{-14} * z + 2.644e^{-27}} \quad (19)$$

The equation (19) is to be simulated and implemented onto the FPGA. The step response is shown in Fig. 14 created by ModelSim.

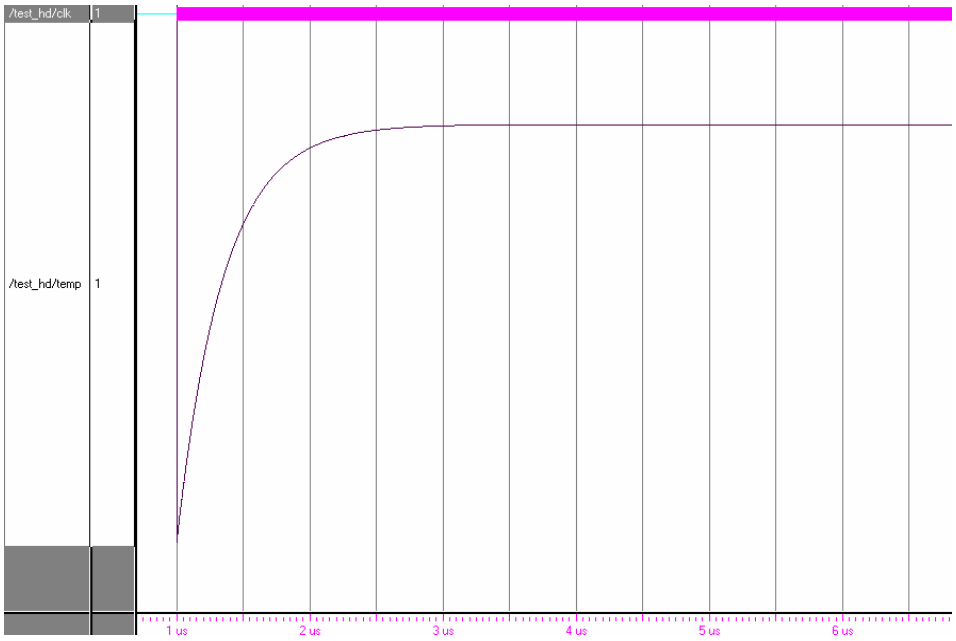

Fig. 14 The step response of equation (19) created by ModelSim

4. Conclusions

Tremendous improvements are obtained in implementing the system design onto the FPGA device. The overshoot in the FPGA design has zero percent. A very fast response to a step input giving the rise time of 0.763μs. The settling-time has been reduced to 1.367μs. The results, in case of hard disk drive system are very encouraging to design, simulate and implement the higher order complex control systems onto the FPGA, so that the System-On-Chip (SOC) can be developed.

REFERENCES

1. Richard C. Drof and Robert H. Bishop, *Modern Control Systems*, Addison-Wesley, Eighth edition, 1999.
2. Wei Zhao, Byung Hwa kim, Amy C. Larson and Richard M. Voyles *"FPGA implementation of closed loop control system for small scale robot"*. In Proceedings, 12th International conference on advanced robotics-ICAR 05, pages 70– 77, 2005.
3. Y. F. Chan, M. Moallem, W. Wang, *"Efficient implementation of PID control algorithm using FPGA technology"*, Proceedings of the 43ed IEEE Conference on Decision and Control, V5, PP. 4885-4890, Bahamas 2004.
4. Xilinx, "Spartan FPGA Family: Complete Data Sheet" 2004. http://www.xilinx.com/bvdocs/publications/ds099.pdf.
5. TeckB.Goh, ZhongmingLi, BenM.Chen, TongHengLee, and TonyHuang, *"Design and Implementation of a Hard Disk Drive Servo System Using Robust and Perfect Tracking Approach"*. IEEE transactions on control systems technology, vol.9, no.2, March 2001.
6. Robert H. Bishop and Richard C. Drof, *"Teaching Modern Control System Design"* Proceedings of the 38th Conference on Decision & Control Phoenix, Arizona USA December,1999.
7. National Instruments: http://www.ni.com. FPGA based control: Millions of transistors your command, 2004.
8. Douglas L. Perry; VHDL Programming by Example; Tata McGraw-Hill 2002 4th Edition.