MCA 2nd Semester Examination, 2023

MCA

(*Advanced Computer Architecture*)

PAPER – MCA-201

Full Marks : 100

Time : 3 hours

The figures in the right hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

GROUP–A

Answer any **five** questions : 2×5

1. What is the difference between linear and non-linear pipeline ?

2. Evaluate $Y = (P \times Q)/(R \times X)$ where P, Q, R, X, Y are memory addresses using zero address instructions.

3. Write any two differences between RISC and CISC.

4. What is Flynn's classification of computer ?

5. State locality of reference property of memory hierarchy.

6. What is arithmetic shift operation ? Give an example.

7. What is MIPS ?

8. What is I/O driver ?

GROUP–B

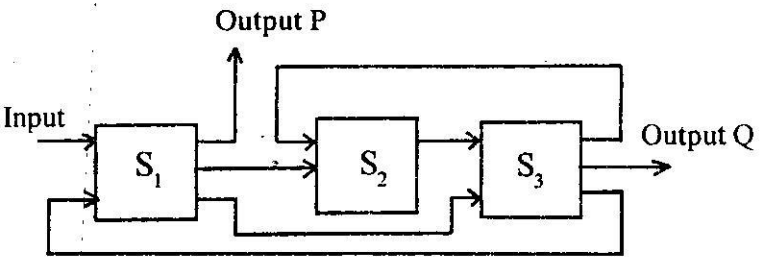
Answer any **four** questions : 15×4

9. (*a*) Explain asynchronous and synchronous models of linear pipelining with a diagram.

   (*b*) What is the application of asynchronous model of pipeline unit ?

   (*c*) What is reservation table with reference to linear pipeline ? Draw a reservation table of a 3 stage linear synchronous pipeline.

(*d*) List all types of connections of the following non-linear pipeline unit : 6 + 2 + 4 + 3



10. (*a*) Explain the terms : Speed up, efficiency and throughput.

(*b*) Derive the maximum Speed up of a *k*-stage pipeline unit.

(*c*) Consider a 5-stage linear pipeline processor with a clock rate of 40 MHz.
Calculate speed up, efficiency and throughput for 20000 instructions. 6 + 4 + (2 + 2 + 1)

11. (*a*) What Von Neumann architecture ? What is its limitation ?

(*b*) Explain hardware control unit with diagram.

(*c*) What is device interface ? How does central computer system connected with peripherals ? Explain with a diagram.

(*d*) Discuss about Programmed I/O mode of data transfer. 3 + 5 + 4 + 3

12. (*a*) Draw and explain MIMD architecture.

(*b*) What is UMA model of multiprocessor ? Discuss with a proper diagram.

(*c*) Compare among UMA, NUMA and COMA model of multiprocessor. 6 + 5 + 4

13. (*a*) With proper diagram, discuss 4-level hierarchical memory organization.

(*b*) What is inclusion property of memory hierarchy ? Explain two polices to maintain coherence property of memory hierarchy.

(*c*) Compare among temporal, special and sequential locality of reference. 6 + (3 + 3) + 3

14. (*a*) What is cache memory ? How can you obtain the hit ratio and average access time ?

(*b*) List advantages and disadvantages of virtual memory ?

(*c*) Explain paging technique with diagram.

6 + 3 + 6

15. Consider the following reservation table of a non-linear pipeline processor for function Q :

		— Clock→					
		1	2	3	4	5	6
Stages	S_1	Q				Q	
	S_2			Q			
	S_3		Q		Q		Q

(*a*) Find out all forbidden an non-forbidden latencies.

(*b*) Obtain the initial collision vector.

(*c*) Draw state transition diagram.

(*d*) List all simple and greedy cycles.

(*e*) Calculate minimal average latency.

$4 + 2 + 5 + 2 + 2$

16. Write short notes on any *three* of the following : 5×3

(*i*) Logical unit of ALU

(*ii*) Associative mapping technique of cache memory

(*iii*) Floating point adder-subtractor arithmetic pipeline

(*iv*) DMA.

[Internal Assessment — 30 Marks]