PG/IIS/ELC/395/22(Pr.)

M.Sc. 3rd Semester Examination, 2022

ELECTRONICS

PAPER – ELC-395

(VLSI Lab)

Full Marks : 50

Time : 3 hours

Answer any **one** question selecting it by lucky draw

The questions are of equal value

Candidates are required to give their answers in their own words as far as practicable

1. Draw half adder circuit using SPICE. From the circuit diagram, obtain the SPICE code of the circuit. Give input and output waveforms of the circuit.

2. Draw DC analysis of the CMOS inverter circuit. Vary width to length ratio (W/L) of the circuit. Give input and output waveforms of the circuit. Use LT SPICE software.

3. Draw schematic diagram of a NAND gate. Obtain the SPICE code from the circuit diagram. Give input and output waveforms.

4. Draw schematic diagram of a NOR gate using SPICE. Obtain the SPICE code from the circuit diagram. Give input and output waveforms of the circuit.

5. Draw layout of an inverter circuit using software. Draw the obtained input and output waveforms.

6. Draw layout of a NAND gate. Obtain the input and output waveforms.

7. Draw layout of a NOR gate. Obtain the input and output waveforms.

8. Write verileg code for full adder circuit. Obtain the input and output waveforms.

9. Write verileg code for $y = \overline{AB + C}$ obtain input and output waveforms.

10. Write verileg code for X-OR gate. Obtain input and output waveforms.

11. Write verilog code for J.K flip-flop and give input-output waveforms.

12. Write verilog code for counter (any type) and give input-output waveforms.

Marks Distribution

Program :	10 marks
Execution :	10 marks
Result :	15 marks
Viva-voce :	10 marks
Laboratory note book :	05 marks
Total :	50 marks