B.Sc.-CBCS/IS/COS/H/C2T/17

2017

COMPUTER SCIENCE

[Honours]

(CBCS)

[First Semester]

PAPER – C2T

Full Marks : 40

Time : 2 hours

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

GROUP–A

1. Answer any *five* questions : 2 × 5

(*i*) Write the truth table of a 3-input X-OR gate.

(*ii*) What will be the representation of $(-19)_{10}$ in 2's complement representation using 8-bit register ?

(*iii*) Capacity of a primary memory is 2 KB. Minimum how many address lines are required to address any memory location ?

(*iv*) What is meant by 'big-endian and little endian' ?

(*v*) What is cache memory ?

(*vi*) What are the i/o data transfer method using memory buses ?

(*vii*) Give an example of zero-address, one -address, two-address and three-address instructions.

(*viii*) What is write-through protocol ?

GROUP–B

2. Answer any *four* questions : 5 × 4

(*i*) (*a*) What is demultiplexer ?

(*b*) Design a 8 × 1 multiplexer using two 4 × 1 multiplexers. 1 + 4

(*ii*) (*a*) Subtract $(1010)_2$ from $(101)_2$ using 2's complement subtraction method.

(*b*) If $(36)_8 = (x)_6$ then find the value of x. 3 + 2

(*iii*) (*a*) Suppose we have a processor that was only 2-address instructions. We need to perform $X = (A + B) * C$ where X, A, B, C are memory locations. Realize the computation using 2-address instruction only for this processor.

(*b*) Briefly mention the stages of instruction execution cycle and role of these stages. 3 + 2

(*iv*) (*a*) Explain the need of memory hierarchy.

(*b*) Draw the memory hierarchy. 3 + 2

(*v*) What is magnitude comparator ? Design one bit comparator and write the truth table, logic circuit using basic gates. 5

(*vi*) Briefly discuss the working of a control unit using a block diagram. 5

GROUP–C

Answer any **one** question from the following : 10×1

3. (*a*) Design a mod-11 binary counter.

   (*b*) Explain Booth's multiplication algorithm. 5 + 5

4. (*a*) How does RISC architecture differ from CISC architecture ?

   (*b*) What is microprogrammed control unit design approch ?

   (*c*) For a memory system, time to access cache memory is 0·5 miliseconds for cache hit and 10·2 miliseconds for cache miss. Cache hit rate is 0·8. Calculate the effective time to access the cache memory. 3 + 4 + 3

[*Internal Assessment* – 10 marks]