PG/IIIS/EL - 2101/09

M.Sc. 3rd Semester Examination, 2009

ELECTRONICS

(*Microprocessor and its Applications*)

PAPER—EL-2101

Full Marks : 50

Time : 2 hours

Answer **Q.No.1** and any **three** questions from the rest

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. Answer *all* questions : 2 x 5

(*a*) Why the falling edge of ALE signal of 8085 CPU is used for latching the AD bus ?

(*b*) Calculate the number of memory chips needed to design 8 K-byte memory if the memory chip size is 1024 x 1.

(*c*) Explain the term: 'Machine cycle' used in microprocessors.

(*d*) Write down the action of the instruction : XTHL.

(*e*) Why register checking does not give the correct result when we use HLT instruction instead of RSTn instruction at the end of the program ?

2. (*a*) What is the difference between Unconditional CALL and Conditional CALL instructions ? Explain with examples.

(*b*) What are the steps that the CPU has to perform when an unconditional CALL instruction is executed ? 5 + 5

3. (*a*) What is the difference between the logical shift and arithmetic shift ?

(*b*) Write down the steps for an arithmetic shift for an 8-bit binary number. Is there any single instruction for the arithmetic shift for a 16-bit number ? 5 + 5

4. (*a*) Explain how the contents of two register pairs BC and DE can be exchanged using stack.

(*b*) Write a program to separate the odd and even numbers available from the ten consecutive memory locations. Assume that the ten numbers available from the locations from 2000 H onwards. After the separation store the results in memory starting from suitable address. 2 + 8

5. (*a*) One output port is designed using one 8-bit D-latch. The D-latch has latch enable input (LE) and one output enable input ($\overline{OE}$). The circuit is shown in *Fig*. (*a*). Find the address of the port.

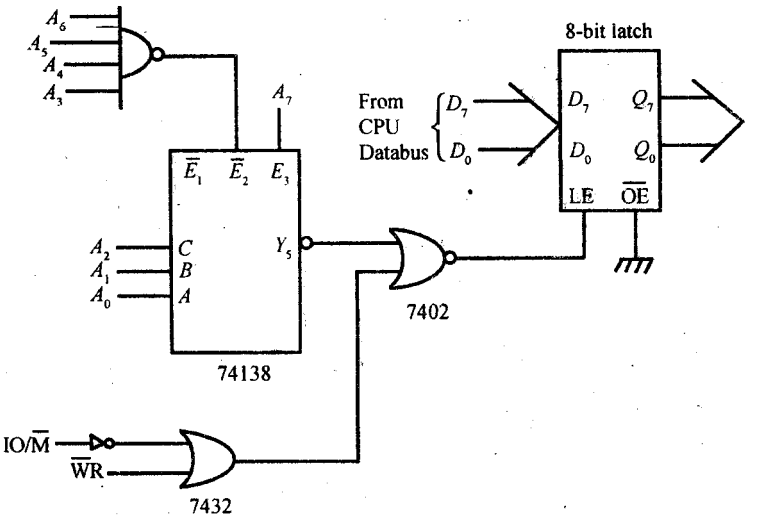

Fig (*a*)

(*b*) The output Q_7 to Q_0 of the latch are connected to the 7-segment common LEDs as shown in *Fig*. (*b*). Write an assembly language program to show 9 on the display.

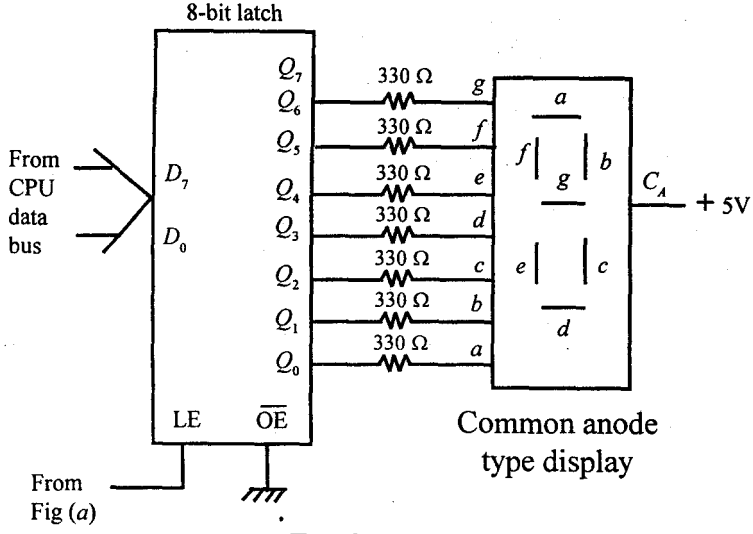

Fig (*b*)

3 + 7

6. One 2K-byte memory is to be interfaced to 8085 CPU so that the starting address of the memory is 8000 H. The memory chip has R / $\bar{W}$ inputs and $\overline{CS}$ input. The data inputs/outputs and address inputs are as usual. 10

[*Internal Assessment* — 10 Marks]