MCA/IIS/203/13

MCA 2nd Semester Examination, 2013

COMPUTER ARCHITECTURE AND ORGANIZATION

PAPER—CS-203

Full Marks : 100

Time : 3 hours

Answer **Q. No. 1** and any **five** from the rest

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. Answer any *five* questions : 2 × 5

(*a*) What is IO mapped input/output ?

(*b*) What are the function of the control unit ?

(*c*) Explain the role of IR and PC register ?

(*d*) Define memory cycle time.

(*e*) What do you mean by cache coherency ?

(*f*) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes ?

(*g*) What is an impedances state ?

2. (*a*) Design an arithmetic circuit for a two register of four bits. The circuit must generate the arithmetic operation is conjunction with the input carry Ci's. Also, give the function table of the above circuit, with brief description.

(*b*) What do you mean by DMA (Direct Memory Access) ? 10 + 2

3. (*a*) Explain the difference between hardwired control and microprogrammed control.

(*b*) A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts : as indirect bit, an operation code, a register code part to specify one of 64 registers, and an address post.

(*i*) How many bits are there in the operation code, the register code part, and the address part ?

(*ii*) Draw the instruction word format and indicate the number of bits in each part.

(*iii*) How many bits are there in the data and address inputs of the memory ?

4 + (3 + 2 + 3)

4. (*a*) What is the difference between direct addressing and indirect addressing ?

(*b*) Draw the block diagram of control unit of basic computer. Briefly explain. 4 + 8

5. (*a*) A digital computer has a memory unit of 64 K × 16 and a cache memory of 1 K words. The cache uses direct mapping with a block size of four words.

(*i*) How many bits are there in the tag, index, block, and word fields of the address format ?

(*ii*) How many bits are there in each word of cache, and how are they divided into functions ? Include a valid bit.

(*iii*) How many blocks can the cache accomodate ?

(*b*) What is EEPROM ? (4 + 4 + 2) + 2

6. Define Von Neumann architecture with proper diagram and explain function of each block. 12

7. (*a*) What is the difference between static RAM and dynamic RAM ?

(*b*) Assume in a program 45% of the instructions are data accessing instruction. The instruction miss rate in 3% and data access miss rate is 16%. Let a hit take 1·5 clock cycle and miss penalty is 95 clock cycle. What is the average memory access time ? 4 + 8

8. Write short notes on : 6 + 6

(*i*) Booth's Algorithm

(*ii*) Addrer-subtractor circuit.

[*Internal Assessment* : 30 Marks]
