MCA/IS/108/13(Pr.)

MCA 1st Semester Examination, 2013

BASIC ELECTRONICS AND DIGITAL LOGIC LAB

(Practical)

PAPER—MCA - 108

Full Marks : 100

Time : 5 hours

Answer any **one** question **(Lottery Basis)**

The questions are of equal value

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. Design NOT, OR, AND, XOR, XNOR gate's using minimum number of NAND gates.

2. Design a circuit to convert BCD to Excess 3.

3. Design a circuit to convert Gray to Binary number and even parity generator.

4. Design NOT, OR, AND, XOR, XNOR gates using minimum number of NOR gates.

5. Design a circuit to convert Binary to Gray code and odd parity generator.

6. Design Full adder and Full subtractor using 8 : MUX.

7. Design Full adder and Full subtractor using 4 : 1 MUX.

8. Design BCD adder using 7483 and NAND gates.

9. Construct clocked SR, D, JK flip-flop using NAND gates only. Verify its operation.

10. Design a four bit 2's complement subtractor using IC 7483 and XOR gates. Show that this circuit is also use as adder.

11. Design ripple counter and using it design mod 3, mod 10 asynchronous counter.

Theory	–	15
Circuit diagram	–	10
Implementation	–	30
Verification	–	15
Lab. Note Book	–	10
Viva voce	–	20