2011

M.Sc.

1st Semester Examination

ADVANCED COM. ARCHITECTURE & MICROPROCESSOR

PAPER—COS-102

Full Marks : 50

Time : 2 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

All notations have their usual meaning.

Module—1

Answer *two* question

1. (a) Describe in detail the pipeline data path along with proper diagram 5

(b) What is vector processor. 3

(c) What are the advantages of pipelining. 2

2. (a) Consider an unpipelined processor that has a 1ns clock cycle and it uses 4 cycles for ALU operation and

branches, and 5 cycles for memory operations. Assume the relative frequencies of these operations are 40%, 20% and 40% respectively. Due to clock skew and setup, the processor adds 0.2 ns of overhead to the clock. How much speed-up in the instruction execution rate will we gain from the pipeline? 5

(b) Consider the following —

Lw R_1, 0(R_2)
Sub R_4, R_1, R_6
And R_6, R_1, R_7
Or R_8, R_1, R_9

Is this program segment safe or hazardous? If any hazard arises to this segment then how can you remove this hazard. 5

3. (a) Difference between the following (any two) : 2.5×2

(i) RISC & CISE;

(ii) Multitasking & Multiprogramming;

(iii) Linear and non-linear pipelining.

(b) What is array processor? Describe any assay processor. 1+4

4. (a) Describe bus architecture technique in vector interrupts (Give an example). 5

(b) Describe Flynn's classification. 5

[Internal Assessment — 05]

Module—2

Answer any *four* questions

1. (a) What is the purpose of the following : 3

(i) MN / $\overline{MX}$;

(ii) $\overline{LOCK}$;

(iii) STOSB / STOSW;

(iv) STD;

(v) ROR;

(vi) AAA.

(b) Describe in brief the software and hardware interrupt of 8086. 4

(c) Draw and explain the timing diagram with the sequence of operation for the interrupt acknowledge machine cycle. 3

2. (a) Connect a 32KB read-write memory with the microprocessor 8086 in the maximum mode configuration from address 58000h. 6

(b) Differentiate between —

(i) 8086 and 8088;

(ii) Microprocessor and Microcontroller;

(iii) Linear and Absolute Decoding;

(iv) Software and Hardware interrupt. 4

3. (a) (i) What is Segmentation? Describe each segment use in 8086 μp. 3

(ii) Describe the following instruction

(i) STI (ii) JB 2

(b) (i) "8237 is a DMA Controller" — Justify your answer. 3

(ii) 8185 I/O port is a handshake mode. Why? 2

4. (a) Describe interval structure of 8254 & how it can act as a timer? 5

(b) (i) Describe the block diagram of 8279. 3

(ii) "8279 is a programmable interrupt controller"— Justify your answer. 2

[Internal Assessment — 05]