2011

MCA

1st Semester Examination

BASIC ELECTRONICS & DIGITAL LOGIC

PAPER—MCA-103

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *seven* questions.

1. (a) Distinguish between a metal an insulator and a semiconductor inlight of band theory. 3

(b) Draw the circuit diagram of bridge rectifier using diodes and briefly explain its operation. 3

(c) What are the advantages of bridge rectifier over full wave rectifier. 2

(d) What is ripple factor. 2

2. (a) Establish the relation $I_c = \beta I_B + (1+\beta)I_{CBO}$. 2

(b) For a transistor $\alpha = 0.998$ and voltage drop across 6kΩ which is connected in the collector circuit is 6 volt. Find the base current for common emitter connection. 3

(c) Draw the circuit diagram showing the fixed bias of an n-p-n transistor in CE configuration. Derive expressions for its stability factors. 5

3. (a) Draw a neat diagram, properly labelled for obtaining the static characteristics curve of a n channel JFET. 3

(b) What are the advantages of FET over BJT. 3

(c) Define "Pinch off voltage" of a JFET. Sketch the depletion region before and after pinch off. (1+1)

(d) Draw the circuit diagram of MOSFET inverter and explain it. 2

4. (a) Write down the characteristics of an ideal OPAMP. 2

(b) Derive the expression for the OPAMP used as a differentiator and draw the circuit diagram. 3+2

(c) What are the advantages of negative feedback over positive feedback. 3

5. (a) Convert the Gray code 101101 into binary code, BCD code and excess 3 code. 3

(b) Represent the following numbers in two's complement form +7 and –7. 2

(c) Design a Gray to Binary code converter. 5

6. (a) Reduce the expression $A\overline{B}C + B + B\overline{D} + AB\overline{D} + A\overline{C}$. 3

(b) What do you mean by cascading of parallel adders? Why is it required? 2

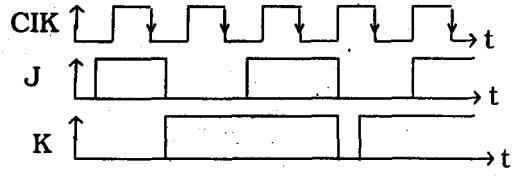
(c) With the help of a logic diagram explain a parallel adder / subtrctor using 2'S complement system. 5

7. (a) Implement the function $F(D, C, B, A) = \overline{C}\overline{B}A + D\overline{C}\overline{A} + D\overline{A}$ using one 8 : 1 Mux and other assorted gates. 6

(b) Design full subtractor using 3 × 8 decoder. 4

8. (a) What is race-around condition? 2

(b) The wave forms shown in figure are applied to the negtive edge triggered JK flip-flop. Draw the output wave forms.



(c) Convert D filip flop to JK flip flop. 4

9. (a) Design with proper circuit diagram synchronous 3bit up-down counter using J-K flip-flops. 4+2

(b) What is the other name of asynchronous counters? Why is that name? 2

(c) What is the modulus of a counter? 2

10. (a) Design and explain 2 bit magnitude comparator. 4

(b) What is the difference between EPROM and EAROM. 3

(c) Write notes on Decimal to BCD encoder. 3

[Internal Assessment — 30]

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