2017

BCA 1st Semester Examination

DIGITAL ELECTRONICS LAB.

PAPER—1197 (Set-II)

(Practical)

Full Marks : 100

Time : 3 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *two* questions taking *one* from each group (lottery basis). 2×30

Group–A 1×30

1. Design a half adder using NOR gates and also design full adder using two half-adders.

2. Design a 1 : 4 DEMUX and verify its truth table.

3. Design a half subtractor using NAND gate and also design a full subtractor using two half-subtractors.

4. Design a circuit to convert BCD to excess-3.

5. Design a 2 bit comparator and verify the truth table.

6. Design a 3 to 8 decoder and verify its result.

7. Design XOR, XNOR and OR gates using NOR gates only.

8. Design an excess-3 to BCD converter circuit and verify its truth table.

9. Design a 4 : 1 MUX using NOR gates and verify the truth table.

10. Design a half subtractor using NAND gates and verify the truth table.

11. Design basic gates using minimum NAND gates.

12. Design a full adder using NAND gates only and verify the truth table.

13. Implement $Y = (X + 2), (\overline{X} + Y)$ using basic gates and verify its truth table.

14. Design a full adder using NOR gates only and verify the truth table.

15. Design gray code to BCD converter and verify the truth table.

Group–B

1×30

1. Design a D F/F using NAND gates and verify its output.

2. Design a asynchronous up counter of MOD 5.

3. Design a 4 bit bidirectional shift register.

4. Design a ripple counter using J-K F/F.

5. Design a 4 bit bidirectional shift register.

6. Design a clocked SR and J-K F/F with preset and clear using NAND gates only.

7. Design AND and OR operation using DTL and establish its truth table.

8. Design J-K master slave F/F and verify its execution table.

9. Design 4 bit ripple counter using J-K F/F.

10. Design OR operation using DTL and establish its truth table.

11. Design and implement right shift register and verify the output.

12. Design asynchronous up-counter of MOD 10 counter.

13. Construct as table multivibrator using IC 555 timer. Measure its frequency and duty cycle by CRO.

14. Design 4 bit SISO register using D F/F and verify the output.

15. Construct clocked S-R F/F using NAND gates verify its operation.

Viva — 05 Marks

PNB — 05 Marks

Internal Assessment — 30 Marks

———