NEW

2016

BCA

1st Semester Examination

DIGITAL ELECTRONICS LAB

PAPER—1197 (Set-1)

(PRACTICAL)

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *two* questions
taking *one* from each group (Lottery basis) 2×30

Group—A 1×30

1. Design Basic gates using minimum number of NAND gates.

2. Design a half adder using NAND gates and verify the truth table. 30

3. Design a 4 : 1 MUX using the NOR gates and verify the truth table.

4. Design a circuit to convert BCD to Excess–3.

5. Design a full subtractor using NOR gates and verify the truth table.

6. Design a 4 × 1 MUX using minimum number of NAND gates and verify its truth table.

7. Implement $Y = AB + AC + B\bar{C}$ using NAND gates and verify its truth table.

8. Simplify the following function using K-map

$$\sum m(0, 5, 7, 13, 14, 15)$$

9. Design 2 bit comparator circuit using suitable gates and verify its truth table.

10. Design 8 to 3 encoder circuit and verify its result using only Basic gates.

11. Implement X-OR, X-NOR, NOR and OR gates using NAND gates only and verify the truth tables. 20+10

12. Design a half adder using only NAND gates and a full adder using two half adders. 15+15

13. Design a 8 to 3 encoder and verify its result using 2 input basic gates. 30

14. Implement $W = \overline{XY} + X + \overline{Y + Z}$ using only NAND gates and verify its truth table. 30

15. Simplify the following function using K-map 30

$$\sum(3, 4, 5, 7, 9, 13, 14, 15)$$

and implement using basic gates.

16. Design 3 to 8 decoder and verify its result. 30

17. Design an excess 3 to BCD converter and verify its truth table. 30

18. Design a Gray Code to BCD converter and verify the truth table. 30

19. Design a 8 : 1 Multiplexer and verify its truth table. 30

20. Design a 2 bit comparators and verify its truth table. 20+10

Group—B 30×1

1. Design S-R F/F using NAND gates.

2. Design asynchronous up counter of MOD 7 counter.

3. Design 4 bit ripple counter using J-K F/F.

4. Design J-K F/F using NAND gates and verify its execution table.

5. Design AND OR operation using DTL and establish its truth table.

6. Design a 4 bit bidirectional shift Register.

7. Design a Buffer register and show the following result.

8. Design asynchronous up counter MOD 5 using suitable gates.

9. Design 4 bit SISO register using D F/F and verify the output.

10. Design J-K master-slave F/F and verify its execution table.

11. Design and implements a right shift resister and verify the operation. 20+10

12. Design AND and OR operation using DTL and establish its truth table. 30

13. Design a 4 bit bidirectional shift register. 30

14. Construct clocked S-R flip-flop using NAND gates and verify its opeartion. 30

15. Design asynchronous up counter of the following MOD using IC 7476 : 30

(i) MOD 10 (ii) MOD 5 (iii) MOD 11

16. Design a J-K master-slave flip flop and verify its execution table. 30

17. Design asynchronous up counter of MOD 7 counter. 30

18. Construct astable multivibrator using IC 555 timer. Measure its frequency and duty cycle by CRO. 30

19. Design a 4 bit SISO register using D flip-flop and verify the output. 30

20. Design a 4 bit ripple counter using J-K flip-flop. 30

INSTRUCTIONS

Distribution of Marks :

Theory	:	*10*
Circuit	:	*05*
Implementation	:	*10*
Verification	:	*05*
Total	:	*30*

Viva	—	*05*
PNB	—	*05*

[Internal Assessment — 30]