NEW

2016

BCA

1st Semester Examination

DIGITAL ELECTRONICS

PAPER—1104

Full Marks : 70

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer *Q. No. 1* and any *four* from the rest.

1. Answer any *five* questions : 5×2

(a) (i) Convert the following decimal number into BCD $(319.86)_{10}$.

(ii) Convert the following hexadecimal number to its decimal equivalent $(DB59)_{16}$.

(b) What is fan in and fan out?

(c) Multiplexer are called 'Universal logic Module' why?

(d) Reduce the given Boolean expression

$Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C}$.

(e) In what conditions EXOR gate acts as NOT and BUFFER?

(f) What is the difference betweem EPROM and EAROM.

(g) Find the base if $7_n \times 8_n = (38)_n$.

2. (a) Express the function $Y = A + \bar{B}C$ in 3+3

(i) canonical SOP and

(ii) Canonical POS form.

(b) What is full adder? Design and draw the circuit diagram using basic gates only. 5

(c) What is BCD addition connection? Perform BCD addition of 1001 & 0111. 2+2

3. (a) The output of a combinational circuit is defined by the following three functions :

$F_1 = \bar{A}\bar{B} + A\bar{B}C$, $F_2 = \bar{A} + B$, $F_3 = AB + \bar{A}\bar{B}$.

Implement this multiple output function using suitable decoder having active low outputs. 5

(b) Implement the Boolean expression : 4

$$f(x, y, z) = \sum m(2, 4, 5, 7) \text{ by } 4:1 \text{ MUX}$$

(c) Implement the function :

$F(D, C, B, A) = \bar{C}\bar{B}A + D\bar{C}\bar{A} + D\bar{A}$ using one 8 : 1 Mux and other assorted gates. 6

4. (a) Minimize the following function given below using the Karnaugh map:

$f(A, B, C, D) = \sum(1,2,5,6,8,10,15) + d(0,3,7)$

and realize the function using NAND gates 5

(b) Convert D flip-flop to SR flip-flop. 4

(c) What is the difference between decoder and demultiplexer ? 2

(d) Design and explain Decimal to BCD encoder. 4

5. (a) What is register. 2

(b) Draw and explain PISO shift register. 5

(c) Design and explain SR(clocked) flip flop made by only NAND gates. 4

(d) Designs full subtractor using 3×8 decoder. 4

6. (a) Describe successive Approximation Method for A/D converter. 5

(b) What is the advantage of inverted R-2R ladder network D/A converter over R-2R ladder D/A converter. 3

(c) With the help of a neat diagram explain the working of a two port input ECR OR/NOR gate. 5

(d) What are the difference between DTL and TTL? 2

7. (a) Design a synchronous BCD counter using J-K flip-flop. 6

(b) Design a Gray to Binary code converter. 5

(c) What is the diference between latch and F/F? What is hold and set up time? 4

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12. Design a Buffer register and show the following result :

Input = 1010

Output = 1010

13. Design a ripple counter using J-K flip-flop. 30

14. Design a J-K master slave flip-flop and verify its result. 30

15. Design a 4 bit bidirectional shift register. 30

16. Design asynchronous up counter of the following MOD using IC-7476. 30

(i) MOD 10 (ii) MOD 5

17. Design a clocked SR and J-K flip-flop with preset and clear using NAND gates only. 30

18. Design a 4 bit bidirectional shift register. 30

19. Design AND and OR operation using DTL and establish its truth table. 30

20. Construct astable multivibrator using IC 555 timer. Measure its frequency and duty cycle by CRO.