2017

M.Sc.

1st Semester Examination COMPUTER SCIENCE

PAPER-COS-102

Subject Code-26

Full Marks: 50

Time: 2 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(Advanced Computer Architecture)

Answer any four questions.

4×10

1. Consider the reservation table of a three stage pipeline processor.

	— time →							
	1	2	3	4	5	6	7	8
Sı	×					×		×
s_2		×		×	5.00			
S_3			×		×		×	
	s_2	s_2	$\begin{array}{ c c c c c } S_1 & \times & & \\ S_2 & \times & & \end{array}$	$S_1 \times S_2 $	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

__ time -

(Turn Over)

- (a) List forbidden and non-forbidden latencies.
- (b) Construct collision vector.
- (c) Draw state diagram.
- (d) List all simple and greedy cycles.
- (e) Calculate MAL.

2+4+3+1

- 2. (a) Explain control hazard with an example.
 - (b) Explain a technique to reduce control hazard.
 - (c) Compare WAR, RAW and WAW data hazards.

2+3+5

- 3. (a) Define speed up ratio, efficiency and through put of a K stage pipeline.
 - (b) Calculate the maximum efficiency of a K stage pipeline.
 - (c) The time delays of a 4-stage pipeline are 60 ns, 70 ns, 90 ns and 80 ns. The latch delay is 10 ns. Determine clock period and frequency of the pipeline.

3+3+4

- 4. (a) Explain inclusion property of memory hierarchy.
 - (b) Distinguish write-through and write-back policy to maintain coherence property of memory hierarchy.
 - (c) Consider a three level memory hierarchy $(M_1 M_3)$ with effective access time 10.04 μ s as shown below:

Memory level	Access time	Hit ratio		
M ₁ (Cache)	t ₁ = 25 ns	h ₁ = 0.98		
M ₂ (Main Memory)	t ₂ = ?	h ₂ = 0.9		
M ₃ (Disk)	t ₃ = 4 ms	11		

Find out the access time of M₂ (i.e t₂)

- 5. (a) Compare NUMA and COMA model of multiprocessor.
 - (b) Draw and explain UMA model of multiprocessor system.
 - (c) Discuss snoopy protocol of multiprocessor.

3+4+3

6. Answer any two questions:

 2×5

- (a) RISC;
- (b) Carry lookahead adder;
- (c) Locality of reference;
- (d) Structural hazard.

[Internal Assessment — 10 Marks]