2017

MCA

1st Semester Examination

BASIC ELECTRONICS OF DIGITAL LOGIC

PAPER—MCA-103

Full Marks : 100

Time : 3 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *seven* questions.

1. (a) List different types of transistor configurations based on the type of common terminal.

(b) Draw common emitter configuration for both p-n-p and n-p-n transistors.

(c) Explain collector base leakage current and collector emitter leakage current. 2+4+4

2. (a) What is op-amp ?

(b) Write down the characteristics of an ideal op-amp.

(c) Derive the expression for an op-amp used as an inverting amplifier with a diagram. 2+3+5

3. (a) Draw and explain Wein bridge oscillator. Also calculate its frequency.

(b) Explain half wave rectifier with diagram. (3+4)+3

4. (a) Compute the following :

(i) $(11.11)_2 = (?)_{10}$

(ii) $(11011110010)_2 = (?)_{16}$

(iii) $(327)_{10} = (?)_8$

(b) Add two BCD numbers 00011000 and 00101000.

6+4

5. (a) *Draw a circuit diagram* using basic gates for the boolean expression Y = A.B + C.(A + B).

(b) Simplify F(W, X, Y, Z) = $\sum_m$ (0, 2, 4, 5, 6, 7, 8, 10, 13, 15) using K-map. 4+6

6. (a) Implement a full-adder wih a decoter and two OR gates.

(b) Construct a 4 bit binary adder-subtractor. 5+5

7. (a) Design a 32 : 1 multiplexer using two 16 : 1 multiplexers.

(b) Implement F(A, B, C) = $\sum$(1, 3, 5, 6) with a multiplexer. 4+6

8. (a) Differentiate between edge triggering and level clocking.

(b) What is propagation delay ?

(c) Explain J-K Master slave flip-flop with diagram. 3+2+5

9. (a) What is counter ? What is the disadvantage of asynchronous counter ?

(b) Explain Mod–10 counter with suitable circuit diagram.

4+6

[Internal Assessment : 30 Marks]